REMARKS

I. STATUS OF THE CLAIMS

Claims 1-24 are pending in this application. New claim 25 has been added.

No new matter has been added by virtue of this amendment.

II. Claim Rejections under 35 U.S.C. §102 and 35 U.S.C. § 103(a)

(i) Claims 1-24 are rejected under 35 U.S.C. §102(e) as being anticipated by or, in the alternative, under 35 U.S.C. §103(a) as obvious over U.S. Patent No. 5,576,557 to Ker et al. ("the Ker patent").

In response, Applicants respectfully submit that at the very least, claims 1, 12 and 19 are patentably distinct and patentable over Ker.

Claims 1 and 19

For example, with respect to claims 1 and 19, Applicants contend that Ker does not teach or suggest, for example, a semiconductor device or a method of forming a semiconductor device wherein *an insulating region inside a second well having a first-type diffusion region along with a first-type diffusion region of a first well constitute a bipolar junction transistor which operates in a cut-off mode and cuts off current from flowing from the first well to a third well*, as essentially claimed in claims 1 and 19.

In formulating the rejection of claims 1 and 19, the Examiner relies primarily on Ker's teachings in FIG. 2, contending that Ker teaches a semiconductor device wherein:

> . . . the insulating region 22 inside a second well, having a first type diffusion region N+ (with Rw2) along with the first type diffusion region N+ (with Rw3) region of the first well 23 constitute a bipolar junction transistor which operates in a cut-off mode and cuts off current flowing from the first well 23 to the third well 21. **(See pages 2 and 8 of the Final Office Action).**

The Examiner further contends that the P-substrate (20) of the semiconductor device in FIG. 2 of Ker essentially forms a "P-well", wherein the Examiner interprets the claimed "second well" of claims 1 and 19 as being the P-substrate (20) of Ker (see, pages 3 and 9 of the Final Action.

In view of the above, the Examiner essentially finds that Ker discloses in FIG. 2 a BJT by the N-well (23) / P-substrate (20) / N-well (22), which can operate in a cutoff mode to cutoff current flowing from a "first well" (interpreted as the N-well (24) in FIG. 2 of Ker) to a "third well" (interpreted as the N-well (21) in FIG. 2 of Ker).

However, Applicants respectfully submit that the Examiner's reliance on FIG. 2 of Ker as teaching a BJT formed by N-wells (20) and (23) is wholly misplaced, and that there is simply no teachings in Ker, either expressly or inherently, that could support the Examiners' findings in this regard.

For example, the N-well (23) and N-well (22) in FIG. 2 cannot constitute a BJT because the wells (23) and (22) are *separated* from each other and in different regions of the circuit. In general, one of ordinary skill in the art readily understands that in order to form an NPN BJT, for example, an N region (emitter), P region (base) and an N region collector) need to be adjacent and in proximity to each other. However, at the very least, Ker does not teach that the N-wells (22) and (23) are proximately adjacent to one another so as to form part of a BJT. Indeed, this is readily gleanable from Ker's teachings in, e.g., Col. 7, lines 60 ~ Col. 9, line 5, and as illustrated in FIGs. 1, 2 and 3.

Indeed, Ker illustrates in FIGs. 1-3 that N-well (23) is clearly separated from the N-well (22). In particular, the symbol "S S" (squiggly line) in Fig. 2 of Ker schematically indicates that there is a *significant separation* between the N-wells (22)

and (23). Moreover, FIG. 3 undoubtedly illustrates that N-well regions (22) and (23) are formed in separate regions on opposite sides of the pad (2). In fact, Ker expressly teaches that in FIG. 2, there is a first pair of neighboring N-type well regions (21) and (22) on the right side of the substrate (20) and a second pair of neighboring N-type well regions (23) and (24) located on the left side of the substrate (20). **In this regard, Ker does not characterize the N-wells (22) and (23) as being neighboring N-wells.**

Therefore, in view of these teachings, irrespective of whether or not the N-wells (22) and (23) are connected by an intervening portion of the P-substrate (20), it is impossible for the regions 22/20/23 to operate as an NPN BJT, as the length of the P-region (portion of P-substrate) between the N-well (22) and N-well (23) is clearly too long for electrons (carriers) to flow from one of the N-wells (22 or 23) to the other N-well (23 or 22) (flow from emitter to collector) through the portion of P substrate (20) (base) between the wells (22 and 23).

The fact that the N-wells (22) and (23) in FIG. 2 of Ker do not form a BJT together is further supported by the fact that none of the BJT's discussed in Ker includes both well (22) and well (23) as part of the same BJT. Specifically, Ker discusses only four possible BJTs referred to as Q1, Q2, Q3, and Q4, respectively, where:
Q1 is formed by a P-type region (25), N-well region (21) and P-substrate (20);
Q2 is formed by N-well region (22), P-substrate (20) and N-well region (21);
Q3 is formed by P-type region (27), N-well region (23) and P-substrate (20); and where
Q4 is formed by N-well region (24), P-substrate (20) and N-well region (23). **(See Column 8, lines 22-Column 9, lines 1-5 of Ker).**

In this regard, Ker does not teach that N-wells (22) and (23) in FIG. 2 of Ker form part of the same BJT structure, as erroneously characterized in the Final Office Action. In fact, given that Ker expressly teaches that N-well (22) is part of Q2 and that N-well (23) is part of Q3, FIG. 1 clearly shows that BJTs Q2 and Q3 are formed in separate regions (100) and (200). These express teachings of Ker further refute the Examiner's inherency theory.

Therefore, for at least the reasons set forth above, Ker at the very least fails to teach or suggest, expressly or under any theory of inherency, a semiconductor device or a method of forming a semiconductor device wherein *an insulating region inside a second well having a first-type diffusion region along with a first-type diffusion region of a first well constitute a bipolar junction transistor which operates in a cut-off mode and cuts off current from flowing from the first well to a third well*, as essentially claimed in claims 1 and 19.

Claim 12

Moreover, Furthermore, Ker also at the very least fails to teach or suggest a semiconductor device which includes an insulating region which is a sub-N-well embedded within a first P-well and having an N-type diffusion region that receives an off mode control voltage for preventing a latch-up current, as essentially recited in claim 12.

In the instant Office Action, the Examiner alleges that N-well (22) of Ker includes a first type diffusion N+ (with Rw2) and that this is the equivalent of the insulating region having an N-type diffusion region, as recited in claim 12. However, even assuming, *arguendo*, that the Examiner's characterization is this regard is correct, Ker

clearly fails to teach or suggest that the diffusion region N+ of the N-well (22) receives an off mode control voltage for preventing a latch-up current, as essentially recited in claim 12.

In contrast, Ker describes connecting the diffusion region N+ of the N-well (22) to an I/O buffering pad 2. In Ker, the I/O buffering pad 2 is connected to the N+ diffusion of N-Well (22) of the semiconductor device. However, the I/O buffering pad 2 connected to the N+ diffusion region of N-well (22) of Ker is clearly not the same feature as an insulating region which is a sub-N-well embedded within a first P-well and having an N-type diffusion region that receives a control voltage and this fact would be readily understood by one skilled in the art. Rather, these I/O pads 2 in Ker, do not provide a control voltage to the diffusion region N+ of the N-well (22), as required by claim 12, but rather, the I/O buffering pads 2 of Ker are connected to lead pins of an IC device so that paths can be set to conduct away undesirable currents caused by ESD. **(See Column 4, lines 10-33 and Figs 1 and 2 of Ker).**

Consequently, as the semiconductor devices and methods of Ker are different from those recited in claims 1, 12 and 19 of the presently claimed invention for at least the reasons discussed above

Thus, for at least the reasons set forth above, claims 1, 12 and 19 are clearly not anticipated by Ker. Moreover, all pending claims that depend from claims 1, 12, and 19 are patentably distinct and patentable over Ker for at least the same reasons given for respective base claims 1, 12, or 19. Accordingly, withdrawal of the anticipation rejections is respectfully requested.

Moreover, new claim 25 is also patentable over Ker for at least the reasons set forth above with regard to claim 1.

III. CONCLUSION

For the foregoing reasons, applicants respectfully submit that the instant application is in condition for allowance. Early notice to that end is earnestly solicited.

If a telephone conference would be of assistance in furthering prosecution of the subject application, applicants request that the undersigned be contacted at the number below.

Respectfully submitted,

Dated: 12/9/07

By: _____

Scott L. Appelbaum
Reg. No. 41,587
Attorney for Applicants

F. Chau & Associates, LLC
130 Woodbury Road
Woodbury, NY 11797
Tel: (516) 692-8888
Fax: (516) 692-8889